Chip Errata
68341 Integrated Processor
3/28/96

This errata list applies to the following 68341 mask sets:

Mask	Processing Geometry	Part Number Suffix
0F23F	0.65u	(none)

The mask set for each part is encoded into the device topside markings - for example, the following markings would indicate a device from the E41R mask, manufactured in the 12th week of 1994:

XC68341FT16
E41R
QEAQ9412

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0F23F
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1. **SIM External Clock with VCO Mode:**

   a) When the external clock with VCO mode is implemented with an XFC capacitor in the 0.01-0.1uF range, the SIM may not reliably detect VCO lock on powerup. As a result, the part never releases the RESET signal even though the EXTCLK input clock and CLKOUT are in phase.

   Workaround: Use a smaller XFC capacitor. For frequencies > 1MHz start with a capacitance value of 10000pf/F_MHz. Example: for 16.0MHz the recommended XFC capacitance is approximately = 10000pf/16.0 = 625pf. An external POR circuit should be used for all external clock applications to guarantee RESET remains asserted until after VCC stabilizes.

   b) For an external reset after POR, the SLOCK bit may not be set. This is only a problem with the assertion of the SLOCK lock indication. The VCO and CLKOUT remain phase locked to the input clock both during and after the external reset.

2. **SIM EXTCLK to EXTAL coupling:** At higher frequencies (>20MHz) EXTCLK can couple to the XTAL output of the crystal oscillator and dampen out oscillation, causing the crystal oscillator to stop.

   Workaround: Coupling effects can be reduced and/or eliminated by routing the EXTCLK input to avoid the crystal circuitry as much as possible.

3. **SIM 3.3V TDICL Spec:** For 3.3V parts, Spec 27 (Data-In Valid to CLKOUT Low) is 8ns instead of 5ns.

4. **SIM BSW input levels:** The BSW pin requires CMOS drive levels - VILmax=0.2*VCC and VIHmin=0.7*VCC.

5. **RTC Ibat:** During battery backup if VDD rises to above 0.8 volt the current draw (Ibat) will increase. Maximum of 1.5mA.

6. **SIM: Clock Skew in External Clock with VCO Mode:** The skew between the EXTAL input falling edge and CLKOUT output falling edge is specified as +/-5ns. Depending on processing, operating voltage, and input clock frequency the skew may exceed this limit. Current production material is tested at skew limits of +8.5/-5.5ns for 5V product, and +10.5/-7.5 for 3.3V product.

   As noted in the MC68341 UMAD/AD user manual update, the PLL phase locks the falling edges of the EXTAL and CLKOUT clocks, not the rising edge as stated in the manual.

7. **RTC:** The RTC registers cannot be updated because the data becomes invalid before it it is clocked into the part. This renders the RTC to be non-functional. This errata item will be fixed in the next revision of the part.

1. **PIT, Background Mode:** If Background Debug Mode is entered and exited while the PIT is running and the FRZ1 bit in the SIM40 MCR is set, the PIT value may decrement by an extra count, shortening the timeout period. This will typically only affect emulation.

2. **Serial: RTS operation:** In the hardware flow-control mode of operation, the first assertion of RTSx* after enabling the RxRTS bit (MR1 register bit 7) does not have to be done manually. If a FIFO position is available, RTSx* is enabled immediately when the RxRTS bit is set.

3. **DACKx assertion for M68000 bus cycles:** Normal DACK timing for M68000 bus cycles is the same as AS68K. The user's manual and design spec indicate that DACK should have AS timing. DONEx uses the same timing, but was never documented.

